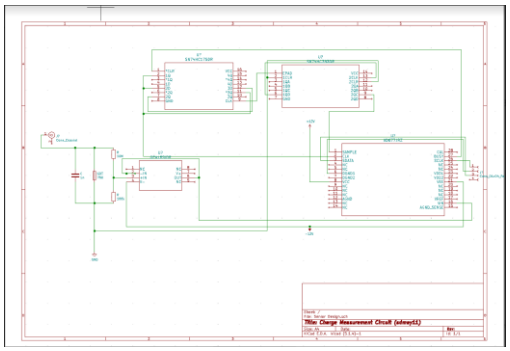
EE/CprE/SE 492 Bi-WEEKLY REPORT 04
2/28/20 – 3/12/20
Group number: sdmay20-11
Project title: Design of a Charge Measurement Device
Client &/Advisor: Jacob Starr/ Long Que
Team Members/Role: Nicholas Wolf – Scribe, Internal Meeting Facilitator – Daniel Frantik, External Meeting Facilitator – Brandon Degelau, Test Engineer – Ben Buettner, Chief Engineer – Keagan Plummer, Report Manager – Colin Ishman

- **Weekly Summary:** For this week, we worked on the Digital schematic and layout. We discussed the different methods to conduct high voltage testing and believe that a breadboard has too high a possibility to arch inside of the board. Perfboard may work for high voltage testing, but there would be a lot of conductors in the board that are not connected. We felt that beginning the PCB will be the safest way to test at high voltages. We also documented our current testing process and discussed how to improve it in the high voltage testing.
- **Past Week Accomplishments:**
  - Discussed High Voltage model design
  - Began Kicad Schematic
    - 
  - Documented Our current testing process
    - Large capacitor charged up. Then hooked into the circuit. This introduces charge into our circuit. The problem is that the large capacitor is dominant in our system. So even though our system was reacting predictably, the test can be improved. Using smaller capacitors have much smaller transients which are harder to measure. We think we have figured out a way to measure it. If we use the single function on the oscilloscope it should allow us to see the small transient and our system capacitor can become the dominant capacitor.
- **Pending Complications:**
- **Individual Contributions:**

Name	Contributions	Hours this Week	Hours Cumulative
Keagan Plummer	Discuss Testing Plan and high voltage model. Work on schematic design.	15	109
Ben Buettner	Discuss Testing Plan and high voltage model. Work on schematic design.	16	109
Nick Wolf	Discuss Testing Plan and high voltage model. Work on schematic design.	12	107

Colin Ishman	Discuss Testing Plan and high voltage model. Document current test plan and improvement ideas.	14	104
Dan Frantik	Discuss Testing Plan and high voltage model. Document current test plan and improvement ideas.	15	110
Brandon Degelau	Discuss Testing Plan and high voltage model. Document current test plan and improvement ideas.	14	109

- **Plans for Upcoming Week:**
  - Finish the Schematic and Layout
  - Order the PCB from Oshpark
  - Discuss ADC testing and GUI design