# Design Of a Charge Measurement Device

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CLIENT: HONEYWELL(JACOB STARR, NATHEN ORTON)

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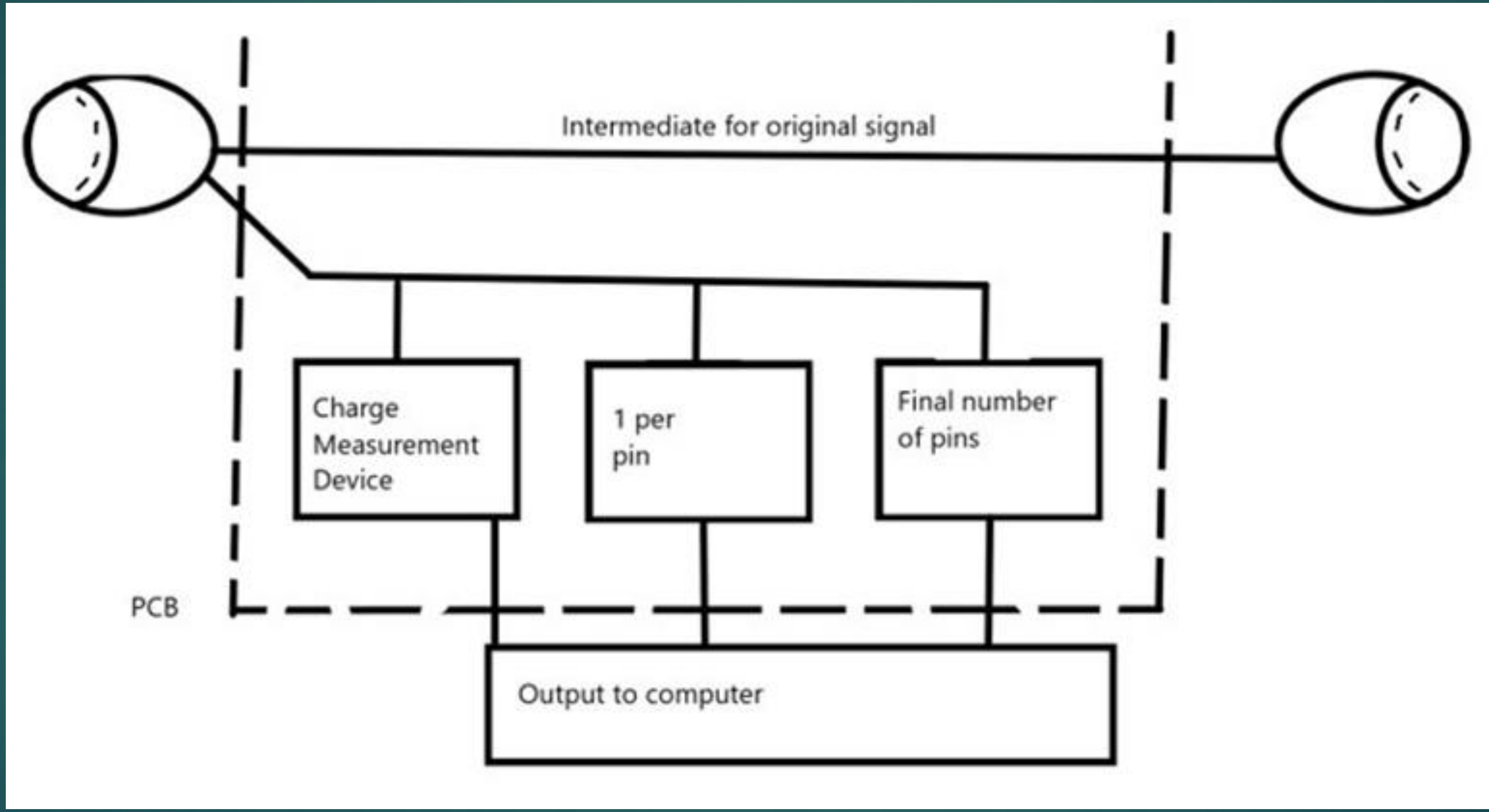
# Problem Statement

- Honeywell needs a way to accurately measure the accumulation of charge on electronic devices they are testing. The circuit should be capable of measuring the electronic discharge between a pin and connector shell while a high voltage is applied to the pin. The desired device should be reasonably sized and capable of handling any conditions or operating points that Honeywell specifies. The application of this device is important for extending Honeywell's ability to accurately test and understand the behavior of the electronics they are developing.

# High Level Overview

- Build a circuit that can measure the amount of charge of a connected device
- Q=C*V
- Charge on the shell should create a voltage across the Capacitor

# Conceptual Sketch



# Functional Requirements

- Measure charges between 10 nC and 300 nC
  - 1 nC accuracy
- Works between 250 V to 750 V
- Create a simple design

# Considerations

- Assumptions
  - Lab based equipment
  - Cost is not an issue
  - Users are knowledgeable about the design
- Limitations
  - Higher accuracy requires higher voltage
  - Limited knowledge of the system design is integrated into

# Potential Risks & Mitigations

- High voltage testing procedure
- Keeping everyone informed about what being worked on before testing the circuit
- Lock out tag out plan

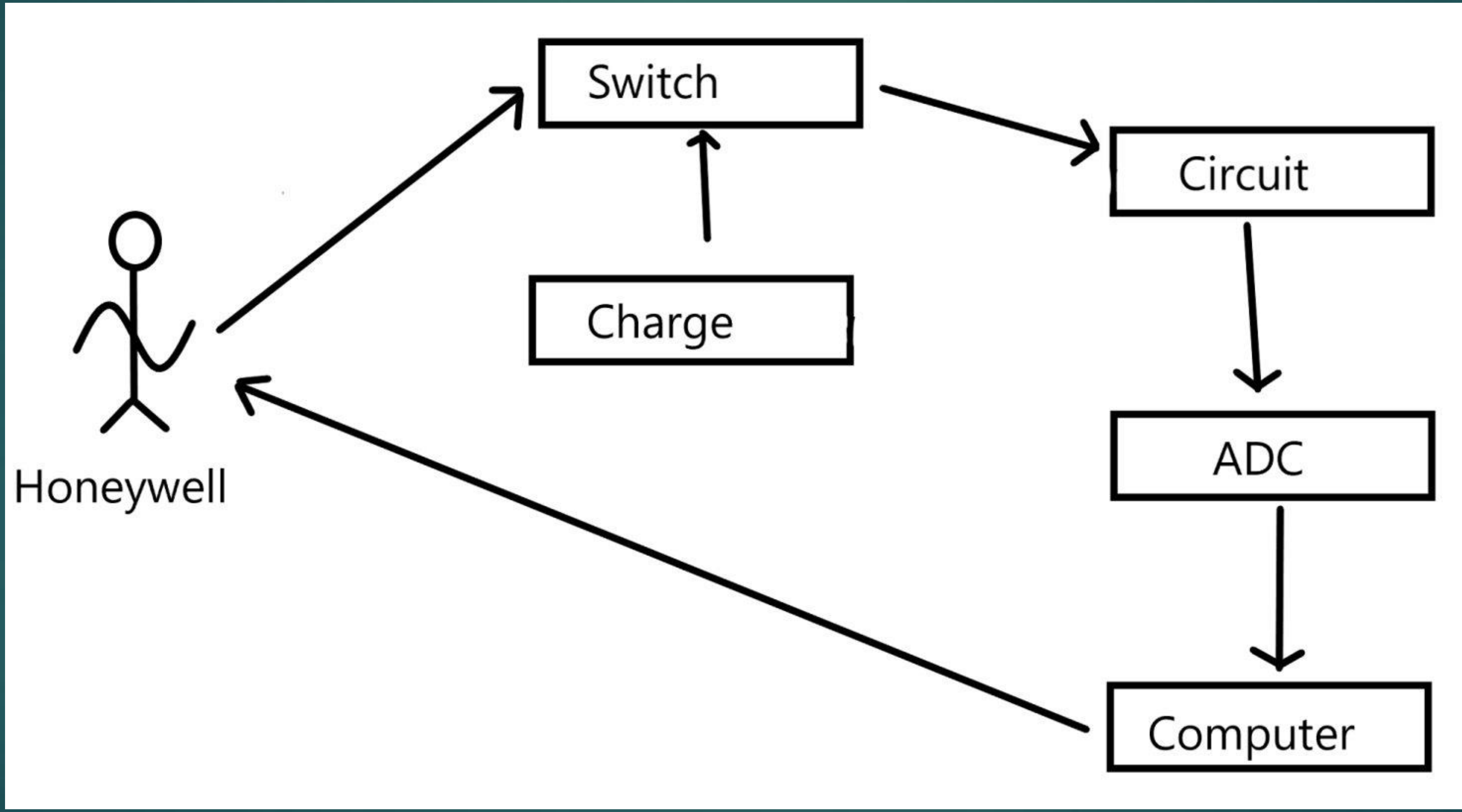
# Resource/Cost Estimation

- Given a budget of $2500 Per semester
  - High Voltage Power Supply was lent to us by Honeywell
  - Spent approximately $400 on components
  - Most for low voltage testing
  - ADC and parts where order for high voltage circuit

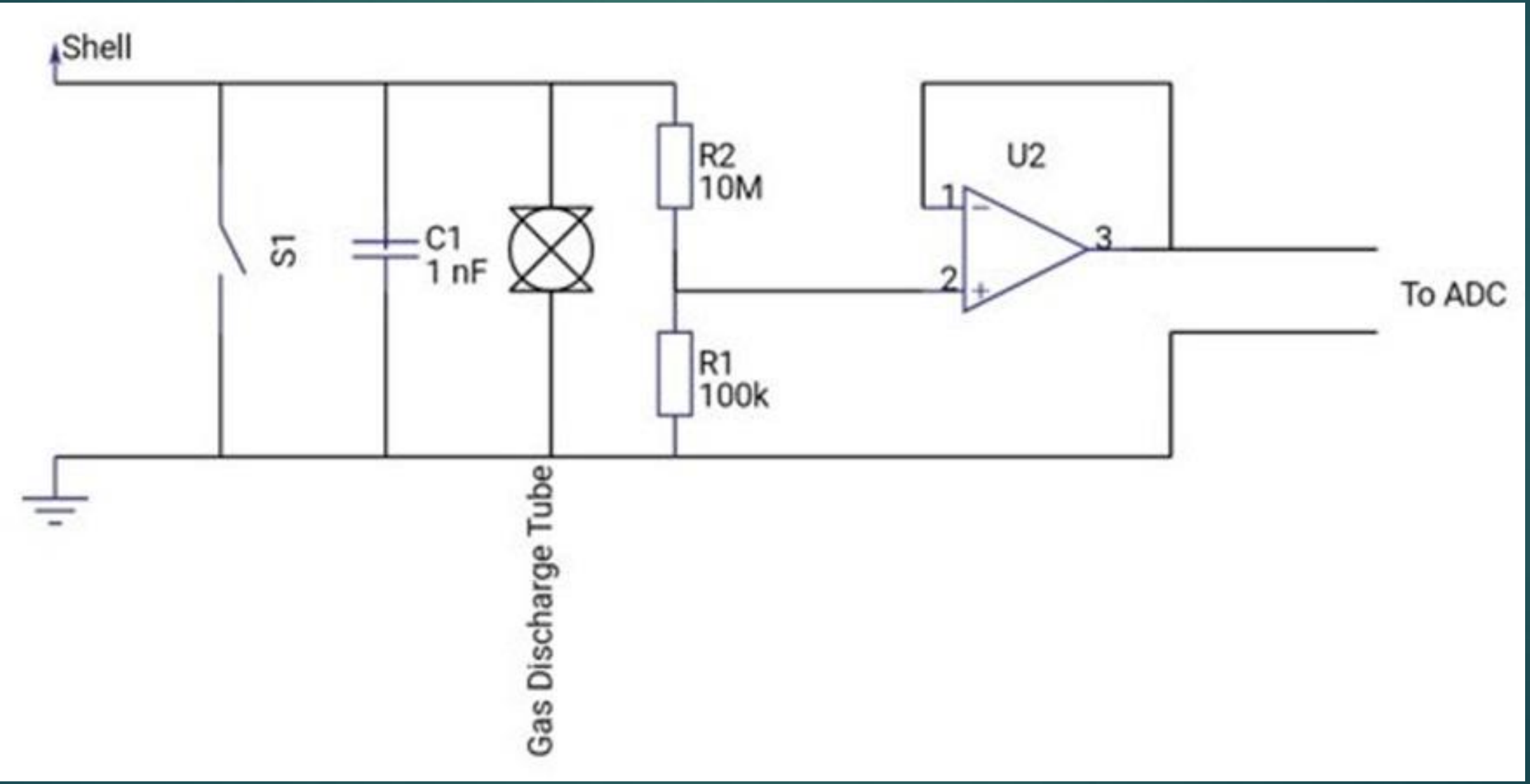
# Milestones and Schedule

| Project Step | Oct | Nov | Dec | Jan | Feb | Mar | Apr |
|---|---|---|---|---|---|---|---|
| Charge Measurement Research | | | | | | | |
| Low voltage model | | | | | | | |
| Part research | | | | | | | |
| PCB design | | | | | | | |
| High voltage model | | | | | | | |

# Functional Decomposition



# Detailed Design



# HW/SW Used

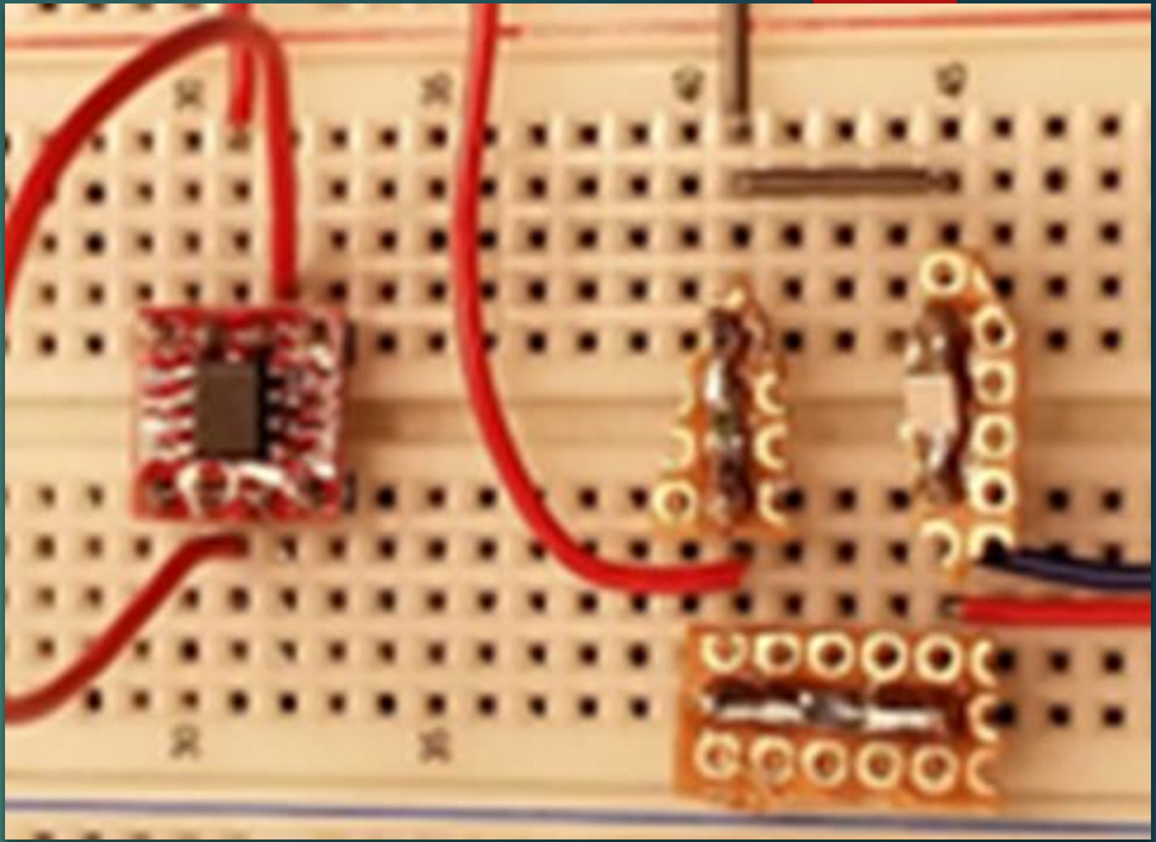
- Before COVID-19 Shutdown
  - Altium Designer
  - Kicad
  - Test Equipment
    - HV power supply, Oscilloscope, Multimeter
- Post COVID-19 Shutdown
  - PSPICE

# Test Plan

- Testing will be divided between a low voltage and high voltage model
  - Low voltage model – breadboard
  - Applying known voltages across known capacitances
  - Tools: Multimeter/oscilloscope
- PSPICE Simulations
  - Confirm design at higher voltages

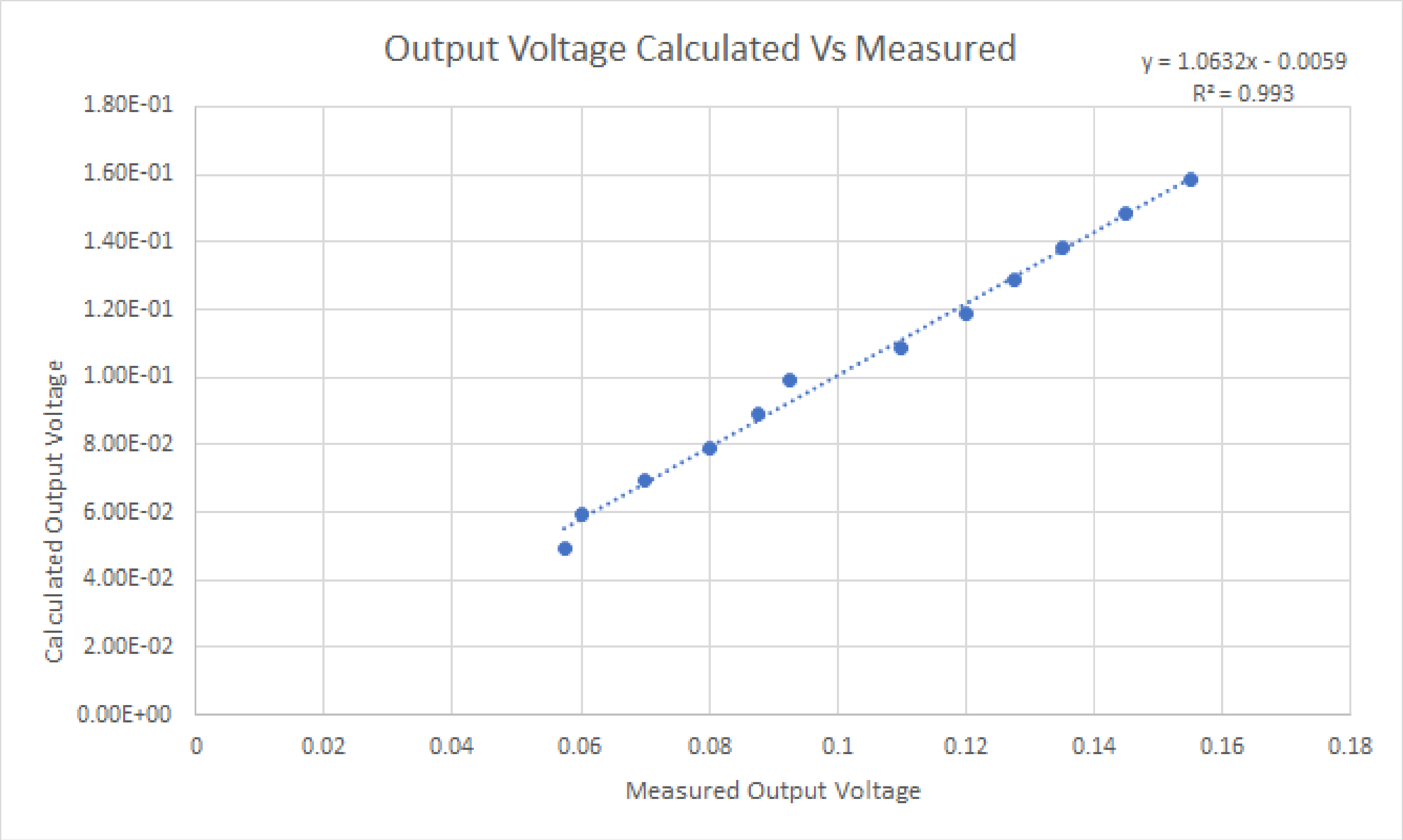
# Physical Prototype

- Low Voltage Model made
  - Made on breadboard
  - Capacitor values
    - Source capacitor: 100 nF
    - Reference capacitor: 1 nF
- Voltage test range 5 – 15 VDC



| | | | | | | |
|---|---|---|---|---|---|---|
| C Charged | 9.89E-06 | 1.00E-09 | | 101 | | |
| | | | | | | |
| Voltage | Voltage Across C1 | Charge On C1 | Measured Voltage Before Op | Measured Output Voltage | Calc Voltage Out | Calc Voltage Before Op amp |
| 5 | 4.997 | 4.94E-05 | 5 | 0.0575 | 4.95E-02 | 4.996494630E+00 |
| 6 | 5.997 | 5.93E-05 | 6 | 0.06 | 5.94E-02 | 5.996393495E+00 |
| 7 | 6.997 | 6.92E-05 | 7.0625 | 0.07 | 6.93E-02 | 6.996292360E+00 |
| 8 | 7.998 | 7.91E-05 | 8 | 0.08 | 7.92E-02 | 7.997191124E+00 |
| 9 | 8.998 | 8.90E-05 | 8.9375 | 0.0875 | 8.91E-02 | 8.997089990E+00 |
| 10 | 9.999 | 9.89E-05 | 9.935 | 0.0925 | 9.90E-02 | 9.997988754E+00 |
| 11 | 10.999 | 1.09E-04 | 10.93 | 0.11 | 1.09E-01 | 1.099788762E+01 |
| 12 | 11.999 | 1.19E-04 | 11.9375 | 0.12 | 1.19E-01 | 1.199778648E+01 |
| 13 | 12.999 | 1.29E-04 | 1.29E+01 | 0.1275 | 1.29E-01 | 1.299768535E+01 |
| 14 | 13.999 | 1.38E-04 | 1.39E+01 | 0.135 | 1.39E-01 | 1.399758421E+01 |
| 15 | 14.999 | 1.48E-04 | 1.48E+01 | 0.145 | 1.48E-01 | 1.499748308E+01 |

# Low Voltage Testing



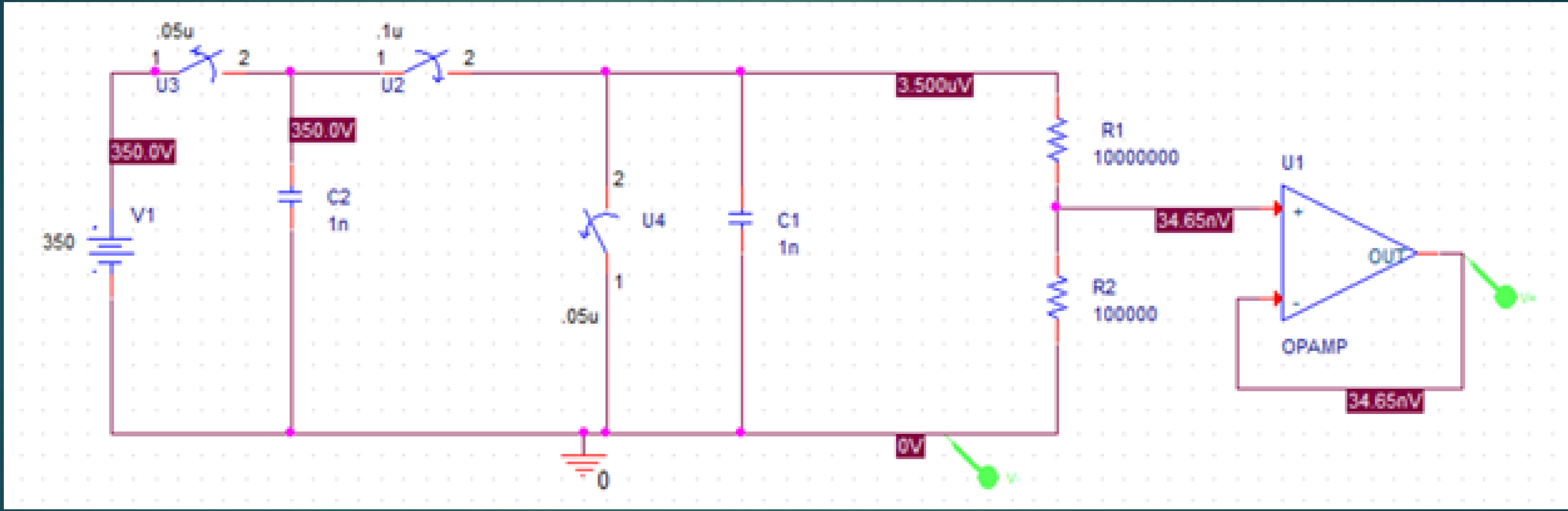
# Low Voltage Testing Conclusions

- $R^2$ Value is 0.993
- System behaving very predictably
- Linear Equation derivable
- Planned to proceed with high voltage testing

# COVID-19

- No access to lab for testing
- No in person meeting
- Used PSPICE to test high voltage model

# PSPICE



.05u
1
2
U3
.1u
1
2
U2
350.0V
350.0V
V1
350
C2
1n
2
U4
1
.05u
C1
1n
3.500uV
R1
10000000
R2
100000
U1
34.65nV
+
OUT
-
OPAMP
34.65nV
0V
0

# PSPICE Continued

| | | | | | | |
|---|---|---|---|---|---|---|
| C Charged | 1.00E-09 | | 1.00E-09 | | 101 | |
| | | | | | | |
| Voltage | Voltage Across C1 | | Charge On C1 | Measured Voltage Before Op | Simulated Output Voltage | Calc Voltage Out |
| 50 | 50 | | 5.00E-08 | | 0.248 | 2.48E-01 |
| 100 | 100 | | 1.00E-07 | | 0.495 | 4.95E-01 |
| 150 | 150 | | 1.50E-07 | | 0.743 | 7.43E-01 |
| 200 | 200 | | 2.00E-07 | | 0.99 | 9.90E-01 |
| 250 | 250 | | 2.50E-07 | | 1.238 | 1.24E+00 |
| 300 | 300 | | 3.00E-07 | | 1.486 | 1.49E+00 |
| 350 | 350 | | 3.50E-07 | | 1.734 | 1.73E+00 |

# PSPICE Conclusions

- Theory of the design confirmed
- Design should be able to be used by Honeywell for their testing

# Engineering Standards and Design Practices

- Engineering Standards
  - IEEE 4-2013 (High Voltage Testing)
  - IEEE 1696-2013 (High Voltage Probe Measurement)
- Practices
  - No official design practices were applied to this project.
  - The main design constraint this project dealt with was ensuring all components would safely operate under the high voltage range designated by Honeywell.

# Member Responsibilities

- Ben Buettner – Test Engineer
- Brandon Degelau - External Meeting Facilitator
- Colin Ishman – Report Manager
- Daniel Frantik – Internal Meeting Facilitator
- Keagan Plummer – Chief Engineer
- Nick Wolf - Scribe

# Conclusion

- Future Prospect of the Project
  - Honeywell wanted a small, easily repeatable circuit they could modify to fit their needs
  - We do not have a physical High Voltage prototype, but
    - The theory behind the design has been confirmed in P-Spice and low voltage testing
    - We believe Honeywell can proceed with this design

# Questions?